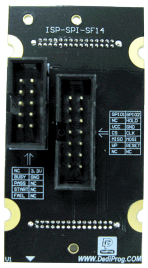
SF700

SPI Flash Programming Solutions Specification

V1.0

The Innovative solution to update the SPI Flash on board and Offline

- **High performances**
- **USB High speed support**
- **In Circuit Programming (program on board SPI Flash)**
- **Socket Programming (program SPI Flash in the socket)**
- **Start Button function**
- **Standalone mode : Update the SPI Flash without computer**
- **Support Single, Dual, Quad and Octal IO (By IC spec)**
- **Three software optimized interfaces:**
  - **Engineering Interface for expert**
  - **Command Line for automated control**
  - **Production interface for operator**
- **Multi-Programmers support through USB**
- **Friendly and powerful tool with free life time update via Website**
- **Portable programmer**
- **Advanced I/O control**



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I. Products Comparison

SF700 is the all-new designed SPI Flash engineering programmer, it supports the major SPI NOR Flash and SPI NAND Flash in the market. SF700 continues to provide the strong engineering mode and command line as SF600 to satisfy the demand from R&D. Apart from the engineering application, SF700 also support project file for small volume production demand. SF700 can do programming in parallel with multiple programmers or standalone mode.

Table1: Feature comparison table

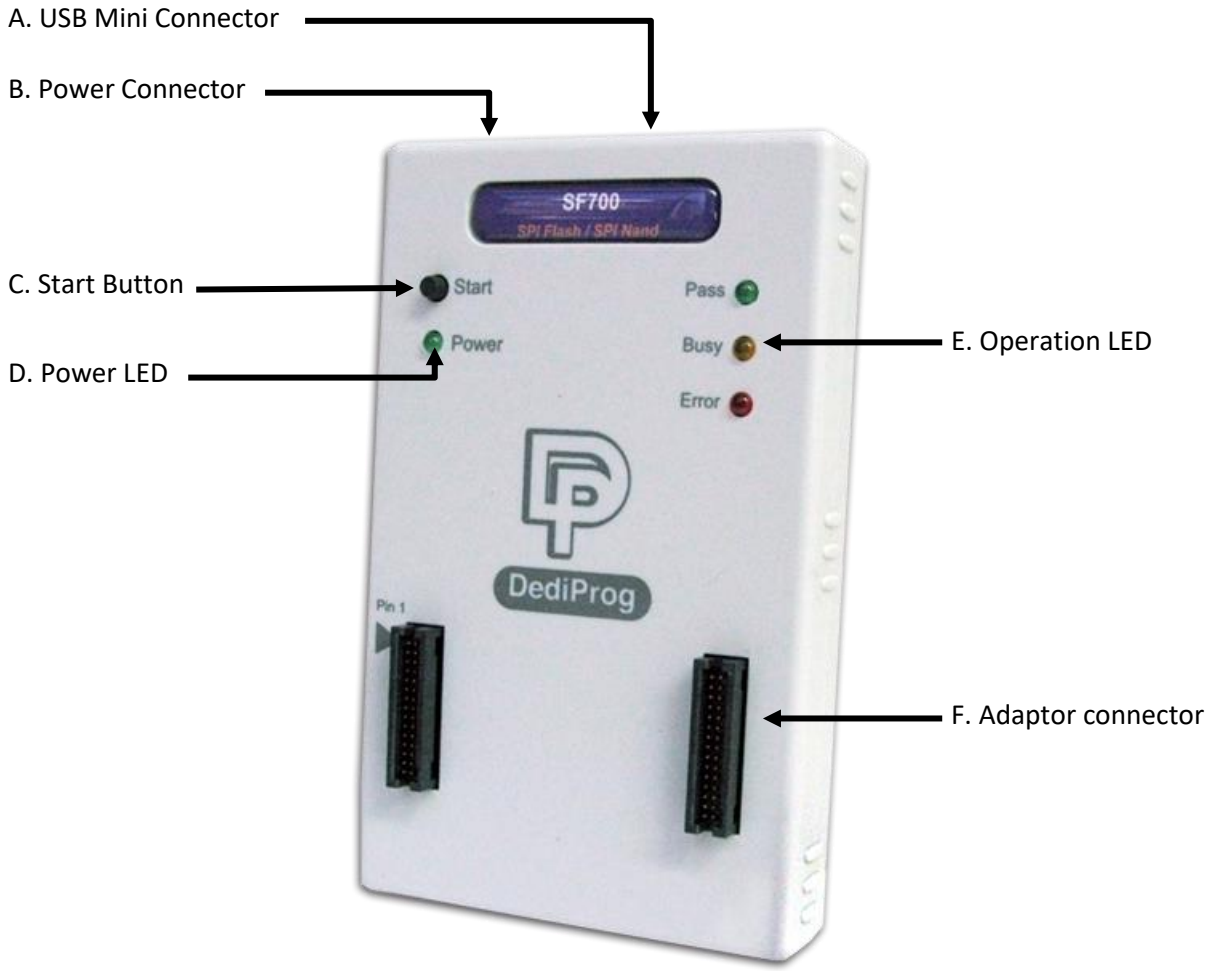
Features	SF100	SF600	SF600*Plus*	SF700
SPI NOR Flash Programming	V	V	V	V
SPI NAND Flash Programming				V ☆
Octal IO				V ☆
Quad IO		V (ICP Port Only)	V (ICP Port Only)	V
Dual IO		V	V	V
Single IO	V	V	V	V
Flash IC VCC: 1.8V/2.5V/3.3V	V	V	V	V
Flash IC VCC: 1.2V				V ☆
In Circuit Programming	V	V	V	V
Socket programming		V	V	V
Standalone mode (Single IO mode only)			V	V
Start Button feature	V	V	V	V
Multi-Programmers in USB Mode	V	V	V	V
Engineering GUI	V	V	V	V
Command Line	V	V	V	V
Production GUI	V	V	V	V
Backup Boot Flash	V	V	V	V
USB 2.0 Full speed	V			
USB 2.0 High speed		V	V	V

II. SF700 Description

SF700 has been designed to offer the best possible performances to program the SPI Flash in different conditions.

2.1 Interface description

Fig 1: SF700 Programmer



A. USB Mini Connector

USB connector is used to communicate with the SF software during the USB mode or to provide the power during the standalone mode.

B. Power Connector

Connect power adaptor to SF700 when executing standalone programming.

C. Start Button

The Start button is operations from the programmer either in USB mode. By pressing and hold 2 seconds the button, the SF700 starts to execute the operation procedures defined in the software Batch configuration in USB mode or in standalone mode. The pre-loaded project is required in standalone mode.

D. Power LED

Power LED is the indicator when SF700 is powered by USB cable or power adaptor.

E. Operation LED

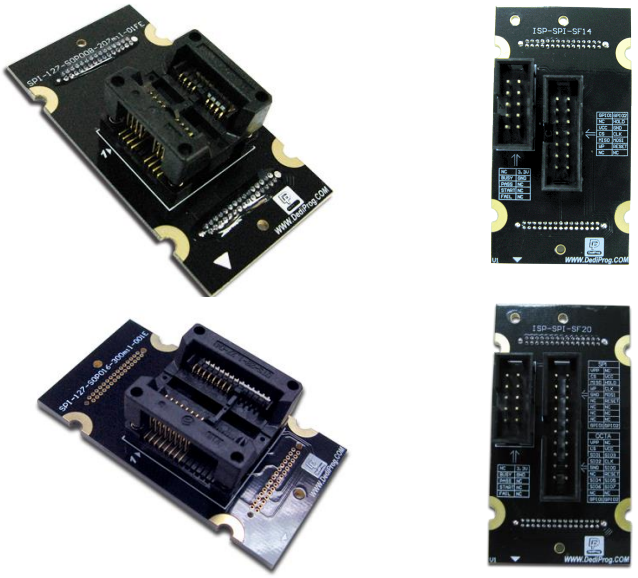
- **Red Led:** Error
- **Orange Led:** Operation is on going
- **Green Led:** Pass

F. Adaptor Connector

For ICP programming (online):
Plug SF700 dedicated ISP adaptor with ICP cable when executing ICP programming.

For socket programming (offline):
Plug the DediProg socket adaptors and program the SPI Flash off line. DediProg is providing different socket adaptors to fit the market SPI Flash packages. Review the socket adaptor available on DediProg website.

Fig 2: Socket adaptors and ISP adaptors



2.2 ISP Adaptor Description

The ISP adaptors with ICP cable are used to program the on board SPI Flash. The flat cable is flexible and convenient to manipulate. It must be kept as short as possible to not impact the signal quality. Even if SF700 strong buffers can provide high capacitance, the communication failure may occur due to weaker driving capability of the on board SPI Flash. In case of communication problems, try to reduce the bus frequency from the software interface.

For customization of the ICP-cable (number of signals, pin out assignment or connector size), please contact DediProg. DediProg is providing additional accessories to fit your target board like:

A. ICP split cable:

You can connect each signal individually according to your own pins assignment.

B. SO Test Clip:

You can connect the SF700 directly on the SPI Flash SO package (SO8N, SO8W, and SO16W)

Table 2: SF700 ISP adaptor pin header description:

ISP Adaptor Model: ISP-SPI-SF20
(Pin compatible with SF600)

1	VPP	(#CS2)	**2**
3	#CS	VCC	**4**
5	MISO(DQ1)	#Hold(DQ3)	**6**
7	#WP(DQ2)	CLK	**8**
9	GND	MOSI(DQ0)	**10**
11	NC	Reset	**12**
13	(DQ4)	(DQ5)	**14**
15	(DQ6)	(DQ7)	**16**
17	NC	NC	**18**
19	GPIO1	GPIO2	**20**

ISP Adaptor Model: ISP-SPI-SF14
(Pin compatible with SF100)

1	GPIO1	GPIO2	**2**
3	NC	#Hold(DQ3)	**4**
5	VCC	GND	**6**
7	#CS	CLK	**8**
9	MISO(DQ1)	MOSI(DQ0)	**10**
11	#WP(DQ2)	Reset	**12**
13	NC	NC	**14**

Table 3: Description of the signals:

Name of the signals	Description
VPP	High voltage applied on the SPI Flash to speed up the programming and erasing operations. (Default disable)
#CS, #CS2	Chip select pins for SPI Flashes. SPI Flash 1 or 2 can be selected from the software.
VCC	VCC is used to supply the power to SPI Flash. The VCC level can be adjusted from the software. A diode protects the SF700 VCC from the application VCC.
MISO(DQ1)	Data out from the application memory (master in slave out) when memory work in single IO mode. Bi-directional when memory works in Dual/Quad/Octal IO mode.
#Hold(DQ3)	Driven high when hold function is inactive. Bi-directional when memory works in Quad/Octal IO mode.
#WP(DQ2)	Driven high when write protect function is inactive. Bi-directional when memory works in Quad/Octal IO mode.
CLK	SPI clock signal
GND	GND is the common ground shared between application and programmer
MOSI(DQ0)	Data in of the application SPI Flash (master out slave in) when memory work in single IO mode. Bi-directional when memory works in Dual/Quad/Octal IO mode.
Reset	Open drain output driven low prior any SF700 operation. Reset can be used to turn on the application isolation circuit or reset the target system in order to drive the SPI bus in High Impedance.
DQ4~DQ7	Bi-directional when memory works in Octal IO mode.
General purpose I/O	General I/O can be used for customization.

III. Programming Methods

3.1 In Circuit Programming

The SF700 programmers has been designed to meet the strong and growing demand of SPI Flash users to program and update the memories soldered on board during development, production, and field manipulation or repairing with high performance and low cost.

SF700 can support dual/quad/octal IO programming offering the shortest programming time even if the application board total capacitance do not permit high frequency.

Before trying to update the SPI Flash soldered on Board, make sure that the SPI controller and the application are compatible with the In Circuit Programming method to avoid any conflict with the programmer.

3.2 SPI bus in High Impedance

The SF700 reset signal can be used to reset the target board and switch the application controller in reset mode. User must check if the SPI bus is released in high impedance during this mode to prevent any conflict between the programmer and the application controller. In this mode, the on board flash is supplied by the application.

3.3 SPI bus isolation circuit

If the application controller does not release the SPI bus in high impedance during reset then an isolation circuit (MOSFET, switch, multiplexer...) must be designed in order to isolate the programmer and SPI Flash from the application controller during the update.

DediProg has published an Application Note and reference schematic to help designers to implement the In Circuit Programming method and will be pleased to answer any of your questions on this subject.

Code programming or Update flexibility:

- For code trials during Research and Development (R&D)
- For Production programming
- For application code update or customization in warehouse
- For repairing or update in the field

3.4 Backup Boot Flash method

SF700 can also be used together with DediProg backup boot flash modules so that it forces the application to boot from the backup flash located in the backup boot flash module instead of the soldered SPI flash on the application which it is disabled. The backup SPI Flash can then be accessed at any time by the SF700 without any possible conflict with the application controller. In this case, SF700 cannot update directly the on

board SPI Flash to avoid conflict with the controller.

Applications:

A. **Development purpose** as the system can boot from the backup Flash for the code trials. Engineer can update safely the backup Flash with new code and without any conflict risk with the application controller.

B. **Repair purpose** as the system can still boot from a backup memory even if the on board SPI Flash is corrupted. The technician can use the application flash update tools after the boot to update the on board SPI Flash.

3.5 Socket Programming

The SF700 has been designed to support the DediProg socket adaptors and offer the socket programming flexibility. Different sockets adaptor are provided to fit the different SPI Flash packages proposed in the market.

A. For development:

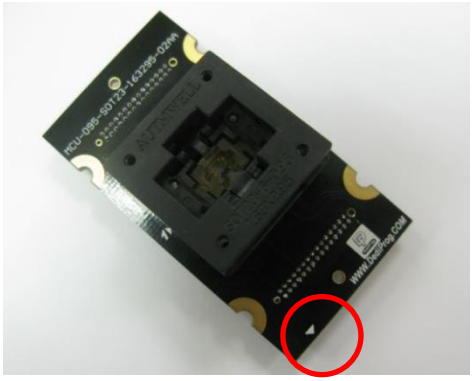
Socket programming can be used during development when an engineering socket is soldered in the target application board so that SPI Flash can be manually removed and programmed in the socket. DediProg supplies engineering sockets which are footprint compatible with the SPI Flash.

B. For Production:

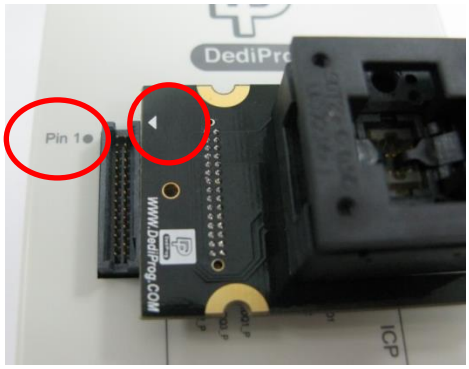
Socket programming can be used to program the SPI Flash before soldering. DediProg software supports multi-programmers through USB to program few SPI Flash in parallel and SF700 also supports Standalone mode.

Note:

The socket adaptor has a white triangle marker on the left and lower side of the socket. Shown as below



To avoid plugging the wrong direction to the socket header, please ensure the marker to aim at the Pin 1 position.



IV. SF700 Software and Standalone Mode

Please refer to latest version SF700 software user manual.

V. Specification

5.1 USB Connector

The USB connector type A is available to communicate with the computer tool or to supply the programmer in Standalone mode. When in Standalone mode, the SF700 has to be supplied through the USB connector or the 5V power jack. This could be achieved by:

- Connecting the SF700 to a computer for the USB power
- Connecting the SF700 to a standard USB Hub (500mA min)
- Connecting the SF700 to the 5V/1A power adaptor through the power jack

USB Power supply specification:

- Vdd = 5V ± 5%
- Idd min = 500mA

5.2 DC and IO characteristics

5.2.1 Socket DC Characteristics

User can adjust the power supply of the target SPI Flash from the software interface. The VCC can be set from 1.2V to 3.8V.

The SPI signals levels are generated according to the VCC selected.

5.2.2 ICP DC and AC characteristics

The ICP connector of ISP adaptor is a 10x2 or 7x2 pin header straight types with 2.54mm pitch. It is used to control the application SPI Flash, and if necessary supply the SPI Flash, provide the high voltage to the SPI Flash, or reset the application chipset, etc.

A. Application SPI Flash supply: VCC

Specification for the ICP connector VCC pin:

- VCC is set at 3.3V by default and can be adjusted down to 1.2V from the software interface
- Icc max supplied = 100mA

The application SPI Flash can be supplied by two different sources:

a) by the programmer via ICP connector VCC pin
b) by the application according to the SPI Flash specification

The SF700 has been designed with a serial diode on the VCC to protect against any conflict with the application VCC.

B. SPI signals management: #CS, #CS2, CLK, MISO, MOSI, DQ2-7, GPIO, Reset

The SPI signals are used to communicate with the application SPI Flash with a high frequency (up to 25MHz). The frequency can be also adjusted from the software interface. The signals are CMOS compatible and are switched in High Impedance when not used. The SPI signals are turned in Low impedance after reset has been driven low.

Table 4: DC specification for SPI signals and IO

Symbol	Parameter	Condition	Min	Max	Unit
Vih	HIGH-level input voltage	VCC=1.2V	0.65*VCC		V
		VCC=1.8V	0.65*VCC		V
		VCC=2.5V	1.6		V
		VCC=3.3V	2		V
Vil	LOW-level input voltage	VCC=1.2V		0.35*VCC	V
		VCC=1.8V		0.35*VCC	V
		VCC=2.5V		0.7	V
		VCC=3.3V		0.9	V
Voh	HIGH-level output voltage	Io=-100uA	VCC-0.11		V
		Io=-2mA	VCC-0.35		V
Vol	LOW-level output voltage	Io=100uA		0.2	V
		Io=2mA		0.35	V

This specification is relative to individual capability of one signal.

ESD high performance protection compliant with IEC61000-4-2 level 4:
15kV (air discharge)
8kV (contact discharge)

Remark: the total capacitance added on the application SPI bus will also depend on the ICP cable length. The ICP cable length must be reduced at the minimum. The SPI flash output buffer capability (MISO) is limited compared to the programmer performances. So even if the programmer is able to drive high capacitance, the SPI Flash soldered on the application will probably not (information read from SPI Flash will be wrong).

C. Smart management of the SPI Flash VCC and SPI signals

In order to minimize the impact of the ICP method on the chipset and application board, the programmer supplies the application SPI Flash with VCC and SPI signals only during the programmer and SPI Flash operations.

Advantages:

a) The programmer is plugged on the application board with VCC OFF and SPI signals in High Impedance to avoid inrush current.

b) All the ICP pins are protected with ESD high performance protections to discharge the Electronics charge before the connection and protect the

application.

c) The SPI Flash VCC and SPI signals are provided only when the user send the command and are switched OFF automatically when the operation is completed. Therefore, the programmer is transparent for the application and can be kept connected during application trials.

D. High voltage supply: VPP/Acc

Specification for the VPP pin

VPP = 5V to 12V

Ipp max = 70mA

The VPP high voltage can be supplied by the programmer and used to speed up programming and erasing of the application SPI Flash if this feature is supported by the SPI Flash supplier.

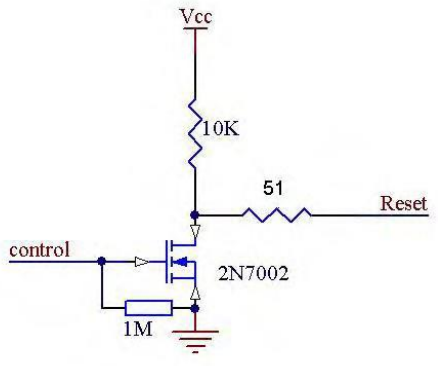
The VPP supply will be applied automatically by the programmer on the VPP pin only during erase, write, or programming operations and only if the VPP option has been enabled on the software. The programmer will also control the VPP voltage level according to the SPI Flash connected and its specification.

E. I/O management: GPIO1, GPIO2, Reset

Two general IO are available on the ICP connector and one Reset for custom needs. The GPIOs and Reset are in High Impedance (HZ) state if there is no software operation ongoing.

Reset: The reset pin is an open drain output which can be used to reset the target system or turn off the isolation circuit.

Fig 3: Circuit diagram:



GPIO: The GPIO signals are in input mode by default. Behavior could be customized.

For the DC characteristics of GPIO1/GPIO2 please refer to the DC table.

ESD high performance protection compliant with IEC61000-4-2 level 4:

15kV (air discharge)

8kV(contact discharge)

5.2.3 ICP timing

The GPIO and Reset have been designed to set the application in programming mode before applying the SPI signal. They can be used to reset the target application, to turn OFF MOSFET and isolate the SPI bus when programmer is working.

A. If No programmer operation is on going
SF700 outputs are equivalent to high impedance.

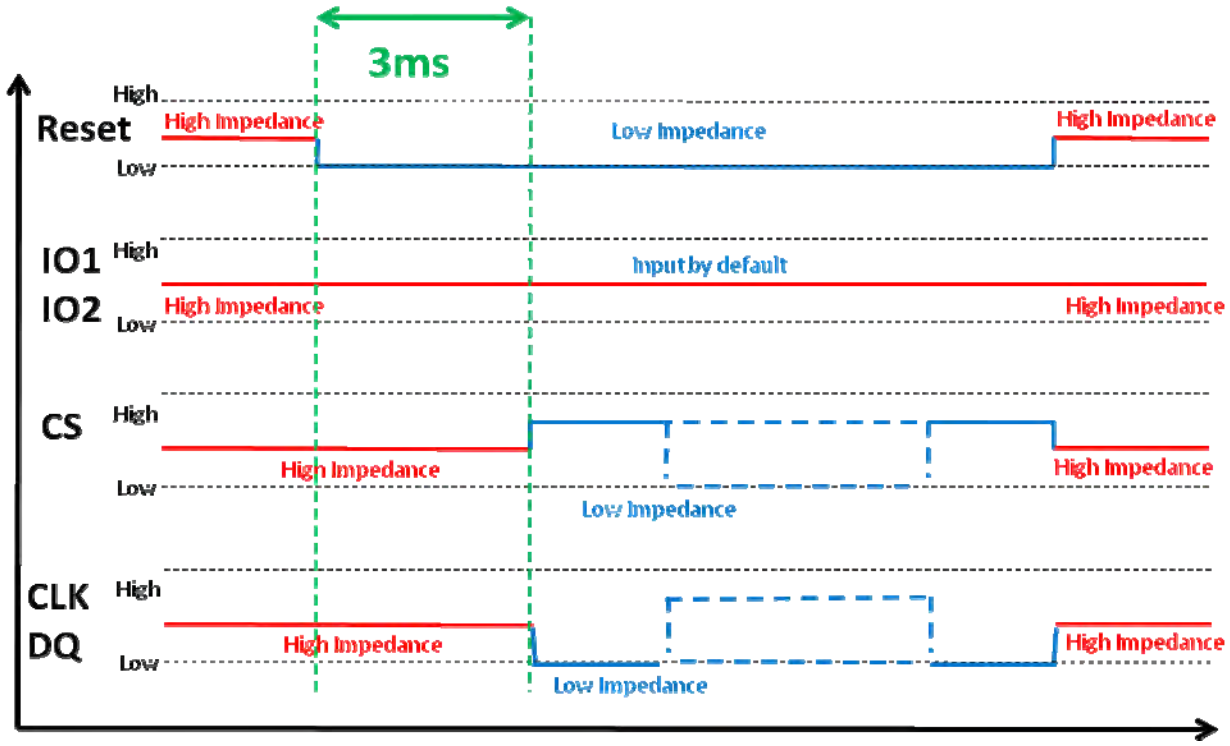
B. When an operation is requested on the user interface
- GPIO1/GPIO2 are kept in Input by default (High Impedance)
- Reset signal is driven Low.

C. 3 ms after Reset is switched to Low Impedance, the SPI outputs are switched in low impedance too.
- #CS and #CS2 are driven high
- Clock and MOSI are driven low
- DQ pins are driven low if Quad or Octal IO mode is enable
- #Hold, #WP are driven High if single IO mode is used

D. The programmer is then ready for the communication with the SPI Flash.
So designer can use the Reset signal to reset or switch the application Serial bus in High impedance. Application controller or circuitry will have a delay of 3ms between Reset is driven low and Programmer SPI outputs are switched from High Impedance to Low Impedance. SPI communication starts 6ms after reset has been driven low.

E. When operation on the memory is finished
The SF700 is switched in High impedance so the application board can boot with SF700 connected without conflict.

Fig 4: IO and SPI timing



5.2.4 Host PC requirements

The SF700 interfaces with IBM compatible PC's through the USB 2.0/1.1 port. This gives full compatibility with the latest PC's, notebooks and portables.

System Requirements:

- PC with Windows XP / Vista / Win7/ Win 8.1/ Win10
- Hard disk with at least 64 MB free space (Depends on SPI Flash capacity).

System Interface:

- PC connection .....USB 2.0/1.1 port

VI. Programming Performance

Table 5: Programming and verify in USB mode

IC Type	IC P/N	Data Size	P+V Time(sec)	
			Engineering mode	Production mode
SPI Octal NOR	MT35XU01GBBA1	128MB	141	138
	MX66UM1G45G	128MB	148	146
SPI NAND	GD5F1GQ4UC	64MB	61	62

SPI CLK setting: 25MHz.

IO Mode: SPI Octal NOR in octal mode and SPI NAND in quad mode.

Please note the programming and verify time will depends on different IC type; please refer to the IC specification before programming.

VII. Revision History

Date	Version	Changes
2019/04/01	V1.0	First release.

DediProg Technology Co., Ltd

Taiwan Headquarter TEL: 886-2-2790-7932 FAX: 886-2-2790-7916
4F., No.7, Ln. 143, Xinming Rd., Neihu Dist., Taipei City 114, Taiwan

China Office TEL: 86-21-5160-0157
Room 518, Building 66, Lane1333, Xinlong Road, Vanke Hongqiao CBD.Min Hang District, Shanghai, P.R.C. 201101

U. S. Office TEL: 1-909-274-8860
209 E Baseline RD, Suite E208 #8, Tempe, AZ, 85283, USA

Technical Support: **support@dediprog.com** Sales Support: **sales@dediprog.com**

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